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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/924,800	08/08/2001	Gary L. Swoboda	TI-33319	2785

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EXAMINER	
BADERMAN, SCOTT T	

ART UNIT	PAPER NUMBER
2113	3

DATE MAILED: 03/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/924,800	SWOBODA, GARY L.	
	Examiner	Art Unit	
	Scott T Baderman	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claim 6 is objected to because of the following informalities: In line 6, "the" (second occurrence) should be "a". Appropriate correction is required.

3. Claim 18 is objected to because of the following informalities: In line 12, "each" should be deleted. Appropriate correction is required.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1-4, 6-9, 11-16 and 18-19 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 4 of copending Application No. 09/920,193. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 4 of the co-pending application includes a plurality of trace leads coupled to portions (trace ports) of the central processing unit, a trace unit coupled to the trace leads (trace ports) for analyzing signals (trace information) from the central processing unit to determine the current activity (it is interpreted that since the trace unit analyzes the signals from the central processing unit, that a memory must be present for storing the signals), a memory for storing a simulation model of the central processing unit (it is interpreted that since the log of activities resulting from operation of the central processing unit are simulated, that this reflects a simulation model), and a processor coupled to the two memories above, wherein the processor determines power consumption for the each activity (via the power consumption values) of the central processing unit. However, claim 4 of the co-pending application does not include the limitation of the central processing unit executing a program, wherein the trace signals are applied as a result of the program execution. A person skilled in the art would have understood that the activities of the central processing unit are a result of executing a program since claim 4 of the co-pending application includes the teaching that the activities are a result of operation of the central processing unit.

As in claim 2, claim 4 of the co-pending application includes that the trace unit determines the current activity (state) of the central processing unit, logs these activities and simulates these activities so that the power consumption can be determined for each activity (interpreted as occurring at each clock cycle) of the central processing unit.

As in claim 3, claim 4 of the co-pending application includes power consumption values for each activity (state) of the central processing unit.

As in claim 4, clam 4 of the co-pending application includes wherein the power consumption values are determined for each activity by simulation techniques.

As in claims 6-9, 11-16 and18-19, the Applicant is directed to the explanation of claims 1-4 above.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Kageshima (6,096,089).

As in claim 1, Kageshima discloses a system for measuring the power consumed by a processing unit processor bus during a predetermined period of time, wherein the system comprises a central processing unit which includes a trace port (Figure 3, column 2: lines 23-29), wherein the central processing unit executes a program and applies trace signals resulting from the execution of the program (Figure 3, elements 1, 3 and 5, column 3: lines 27-40, column 6: lines 51-54). Kageshima also discloses a trace unit for receiving the trace information (element 5 of Figure 3, column 3: lines 27-40, column 6: lines 54-56), a memory for storing the trace information (inherent since the trace information has been "received") (Figure 3, column 3: lines 27-40, column 6: lines 54-56), a memory for storing a simulation model of the central processing unit (i.e., the process of detecting trace information including stall information of the program by use of the processor "operation information" is interpreted as a simulation model) (Figure 3, column 3: lines 27-50, column 6: lines 56-58) and a processor (calculator) for determining power consumption for the program execution of the central processing unit (Figure 3, column 3: lines 59-63, column 6: lines 58-64).

As in claim 2, Kageshima discloses wherein the processor uses trace information applied to the simulation model to determine a state of the central processing unit for each clock cycle (column 3: lines 6-16 and 55-58).

As in claim 3, Kageshima discloses wherein the processor stores parameters identifying the power dissipated for each state of the central processing unit (column 3: lines 55-58).

As in claim 4, Kageshima discloses wherein the parameters identifying the power dissipated for each state is determined by simulation techniques (column 3: lines 41-58).

As in claim 5, Kageshima discloses wherein the central processing unit (for executing the program) and the processor (calculator) are the same processing unit (Figures 3 and 4).

As in claim 6, the Applicant is directed to claims 1-4 above.

As in claim 7, the Applicant is directed to claims 2-3 above.

As in claim 8, the Applicant is directed to claim 4 above.

As in claim 9, the Applicant is directed to claim 1 above.

As in claim 10, the Applicant is directed to claim 1 and 5 above.

As in claim 11, the Applicant is directed to claims 1-3 above.

As in claim 12, the Applicant is directed to claims 2-3 above.

As in claim 13, the Applicant is directed to claim 4 above.

As in claim 14, the Applicant is directed to claims 1-2 above.

As in claim 15, the Applicant is directed to claim 1 above.

As in claim 16, the Applicant is directed to claim 1 above.

As in claim 17, the Applicant is directed to claim 5 above.

As in claim 18, the Applicant is directed to claims 1-4 above.

As in claim 19, the Applicant is directed to claim 4 above.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See Form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott T Baderman whose telephone number is (703) 305-4644. The examiner can normally be reached on Monday-Friday, 6:45 AM-4:15 PM, first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Scott T Baderman
Primary Examiner
Art Unit 2113

STB